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09/458,506	12/09/1999	TAE-GYOUNG KANG	5484-53	8916

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/458,506	KANG, TAE-GYOUNG	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-25 and 29-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-25,33-35,40-45,52 and 53* is/are allowed.

6)☒ Claim(s) *29-32,36-39,46-51 and 54-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 29-32, 36-37, 46-47, 49-50, 54-56 and 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Nagamine (5,534,724) and Bothra et al. (6,020,616).

Regarding claims 29, 33, 34 and 36, APA teaches in figure 10 and related text pages (1-3 and 5-7) a semiconductor device comprising active regions of two or more adjacent transistors having at least more than one first and second electrodes ME2 (figure 9), a plurality of transistor gates P2G (figure 5) disposed between more than one first and second electrodes ME2 of those active regions respectively, wherein two or more gates P2G, P3G are of a predetermined width and length at a substantially identical gap there between, with no intervening structures between the transistor gates.

APA does not teach a substrate and a plurality of dummy gates having a predetermined width and length between and outside ones of the adjacent transistors at a substantially identical gap there between, without intervening transistor gates there between, and wherein a third gap between at least two

dummy gates and an adjacent transistor gate is identical to first and second gaps.

Nagamine teaches in figure 3 and related text a semiconductor device comprising a substrate (column 5, line 10), active regions 16 of two or more adjacent transistors having source and drain regions (column 4, lines 62-65), a plurality of transistor gates 10 on the substrate, wherein two or more gates 10 are of a predetermined width and length (figure 1) at a substantially identical gap there between (figure 4 and column 6, lines 19-24), without intervening transistor and dummy gates there between, on the substrate, and a plurality of dummy gates 20 having a predetermined width and length (figure 1) at a substantially identical gap between adjacent ones of the dummy gates (figure 4 and column 6, lines 19-24), without intervening transistor gates there between.

Bothra et al. teach in figure 3L and related text a plurality of dummy gates 226 (column 5, lines 35-60) having a predetermined width and length formed between and outside ones of the adjacent transistors 204.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form APA's device on a substrate wherein a plurality of dummy gates having a predetermined width and length are formed there between, as taught by Bothra et al., wherein the dummy gates have substantially identical gap there between, without intervening transistor gates there between, as taught by Nagamine, and wherein a third gap between at least two dummy gates and an adjacent transistor gate is identical to first and second gaps, in order to support the device (by providing a substrate there under), to reduce the

inductive noise of the device (by providing a plurality of dummy gates having a predetermined width and length between outside ones of the transistors) and in order to simplify the processing steps of making the device (by providing a substantially identical gap there between and an identical gap between the dummy gates and adjacent transistor gate), respectively.

The combination is motivated by the teachings of Bothra et al. who point out the advantages of forming a plurality of dummy gates having a predetermined width and length between and outside adjacent transistors (figure 3L and column 2, lines 61-67), and by the teachings of Nagamine who points out the advantages of forming a plurality of dummy gates at a substantially identical gap there between as that between the adjacent ones of the transistor gates (column 2, lines 38-41),

Regarding claim 29, APA teaches in figure 5 plurality of active regions each of which having at least one source and drain regions P2S, P2D, and each transistor gate having one or more gate extensions that extend over one of the plurality of active regions between the at least one source and drain regions P2S, P2D and P3S, P3D, respectively.

Regarding the claimed limitations that each of the gate extensions and dummy gate extensions have substantially identical spacing across the substrate, Nagamine teaches dummy gate extensions 226 have substantially identical spacing, and Bothra et al. teach that dummy gate extensions 20 have identical spacing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form APA's device with gate

extensions and dummy gate extensions having substantially identical spacing across the substrate, as claimed.

Note that the claimed limitation of a second gap being substantially identical to a first gap was addressed in previous paragraph. Note further that the dummy gates taught by Nagamine and Bothra et al. can be characterized as being one or more dummy gate extensions. The dummy gate extensions are inherently formed over an inactive regions, since there are "dummy" gates.

Regarding claims 30 and 31, APA teaches in figure 5 a first region (the region above line 62) having plurality of first active regions each having source and drain regions P2S, P2D and P3S, P3D, respectively, and a first portion other than the first active regions, a second region (the region below line 62) having plurality of second active regions each having source and drain regions N4S, N4D and N3S, N3D, respectively, and a second portion other than the first active regions, first and second transistor gates P2G, P3G and N4G, N3G, respectively, are disposed between the source and drain, respectively, and having a first gap there between, and a first metal ME2 (figure 9) connected to the source and drain regions by a plurality of contacts 70, and a second metal 64 connected to a first part of the first metal to supply voltage.

Regarding claim 32, APA teaches in figure 10 a second metal ME3 connected to a second part of the first metal to supply ground voltage (page 7, lines 17-21). APA does not teach a plurality of dummy gates commonly connected to a second

part of the first metal to supply ground voltage. Bothra et al. teach in figure 3L a plurality of dummy gates 226 commonly connected to a ground voltage (column 5, lines 40-50). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the plurality of dummy gates commonly connected to a second part of the first metal to supply ground voltage, as taught by Bothra et al. and APA, in APA=s device in order to suppress the inductive noise of the device. The combination is motivated by the teachings of Bothra et al. who point out the advantages of forming a plurality of dummy gates commonly connected to a ground voltage (column 5, lines 40-50),

Regarding claim 36, APA teaches in figure 5 a plurality of divided gates for a plurality of transistors P2G disposed on active regions. Nagamine and Bothra et al. teach a plurality of dummy divided gates. Forming the dummy divided gates of Nagamine and Bothra et al. in APA's device would substantially fill a region in the substrate, which is devoid of divided gates. Thus, the dummy divided gates and the divided gates form substantially complementary structure, which has a uniform pattern over the substrate, as claimed.

Regarding claim 46, Nagamine teaches in figures 7 and 8 and related text dummy gates 17 having a first portion in contact with a bit line potential supply circuit portion 1 being a bias line, and each dummy gate having at least one second portion extending parallel to the elongated length of the at least two transistor gates. Bothra et al. teach first and second adjacent transistor gates

216 on one and second sides of dummy gates are equidistant from the dummy gates 226.

Regarding claim 49, APA teaches in figure 5 at least more than one gate P2G, P3G of a plurality of transistors respectively have common terminals

Regarding claim 50, APA does not teach a plurality of dummy gates commonly connected. Bothra et al. teach in figure 3L a plurality of dummy gates 226 commonly connected. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the plurality of dummy gates commonly connected, as taught by Bothra et al., in APA's device in order to suppress the inductive noise of the device. The combination is motivated by the teachings of Bothra et al. who point out the advantages of forming a plurality of dummy gates commonly connected (column 5, lines 40-50),

Regarding claims 55-56 and 58-59, it is conventional to reverse the polarity of the transistor. Therefore, it would be obvious to reverse the polarity, as claimed.

2. Claims 48, 51 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), Nagamine and Bothra et al., as applied to claims 46 and 54 above, and further in view of Hansch et al. (6,174,741).

Regarding claims 48, 51 and 57, APA, Nagamine and Bothra et al. teach substantially the entire claimed structure, as applied to claims 46 and 54 above, except stating that the length and the width of the dummy gates are substantially the same as those of the transistor gates.

Hansch et al. teach in figures 3B and 4 the length and width of dummy gates DG, DGL are substantially the same as those of the transistor gates G, GL, respectively.

it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the length and width of the dummy gates substantially the same as those of the transistor gates, as taught by Hansch et al., in the device of APA, Nagamine and Bothra et al. in order to simplify the processing steps of making the device by forming the transistor gates and the dummy gates with the same width and length..

3. Claims 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), Nagamine and Bothra et al., as applied to claims 36 and 37 above, and further in view of Neugebauer (5,748,835).

Regarding claim 38, APA, Nagamine and Bothra et al. teach substantially the entire claimed structure, as applied to claims 36 and 37 above, except a second dimension being a transistor gate width, i.e. a plurality of transistor gates having substantially identical length and width dimensions.

Neugebauer teaches a plurality of transistor gates having substantially identical length and width dimensions (column 13, lines 6-8).
it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of transistor gates having substantially identical length and width dimensions as taught by Neugebauer, in the device of APA, Nagamine and Bothra et al., in order to minimize the error of each of the channel coupled semiconductors when using the device in channel coupled feedback circuits.

Regarding claim 39, the claimed limitation of adjacent ones of the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates, was addressed in detail on pages 6-7.

Response to Arguments

Applicant argues that Nagamine does not teach dummy gates and transistor gates have substantially identical spacing, and Bothra et al. do not teach that dummy lines 226 that are parallel to gate lines 216 have identical spacing.

Claim 29 recites that each of the gate extensions and dummy gate extensions has substantially identical spacing across the substrate. Nagamine teaches dummy gate extensions 226 have substantially identical spacing, and Bothra et al. teach that dummy gate extensions 20 have identical spacing.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form APA's device with gate extensions and dummy gate extensions having substantially identical spacing across the substrate, as claimed.

Allowable Subject Matter

Claims 14-25, 33-36, 40-45 and 52-53 are allowed.

Reasons for allowance

The following is an examiner's statement of reasons for allowance:
Regarding claims 14, 18 and 22, Admitted Prior Art (APA), Nagamine (5,534,724) and Bothra et al. (6,020,616) appear to be the closest prior art reference. APA, Nagamine and Bothra et al. teach substantially the entire claimed structure as recited in claims 14, 18 and 22, except a plurality of dummy gates having the predetermined width and length located between two transistors, as recited in claims 14 and 18, and located not between but to both sides of the two transistors, as recited in claim 22.
Regarding claim 33, Admitted Prior Art (APA), Nagamine (5,534,724) and Bothra et al. (6,020,616) appear to be the closest prior art reference. APA, Nagamine and Bothra et al. teach substantially the entire claimed structure as recited in claim 33, except third and fourth gaps between first and second transistor gates (at an edge of the first and second active regions) and first and second dummy

gates (at an edge of the first and second portions) are substantially identical to each other and to first and second gaps.

Regarding claims 52 and 53, Admitted Prior Art (APA), Nagamine (5,534,724) and Bothra et al. (6,020,616) appear to be the closest prior art reference. APA, Nagamine and Bothra et al. teach substantially the entire claimed structure, as recited in claims 52 and 53, except a plurality of dummy gates having a portion extending in a first direction and a plurality of portions extending in a second direction perpendicular to the first direction. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.
Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
1/13/04

ORI NADAV
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TECHNOLOGY CENTER 2800